Vol. 20 (2026): Proceedings of 2026 International Conference on Materials Science, Energy Engineering and Automation Control (ICMSEAC 2026)
E-ISSN: 3105-0522 P-ISSN: 3105-0514
DOI: https://doi.org/10.70267/mseac.2026116123

Hybrid and Time/Frequency-Domain Approaches for Low-Power High-Performance ADCs/DACs: Recent Advances and Perspectives

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Abstract

The continuous advancement of modern communication systems and sensing technologies has urgently demanded low-power, high-performance Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs). To address this need, this paper presents a systematic review of current optimization strategies, employing literature analysis and architectural comparison to evaluate approaches that aim to balance power efficiency and performance while highlighting their limitations. This review concludes that hybrid architectures and time/frequency-domain methods offer novel perspectives for achieving low-power and high-performance ADC/DACs, with NS-SAR ADCs and TDC-based ADCs identified as particularly promising candidates. Despite numerous proposals to mitigate noise, complete solutions have yet to be realized. Analysis using the Schreier Figure of Merit (FoM) further confirms that high performance and low power consumption remain inherently conflicting objectives. While existing methods have achieved significant improvements in either power efficiency or performance, the development of an ADC/DAC that simultaneously optimizes both metrics remains an open challenge. The insights presented in this review are expected to guide future research on the design of energy-efficient data converters, ultimately supporting the advancement of communication systems, sensors, and other electronic technologies, and contributing to more intelligent and convenient applications in modern society.

Keywords

ADC/DAC, low-power, high-performance, hybrid architecture, time/frequency domain

1. Introduction

Analog signals dominate in nature, while modern electronic systems can only process information in digital form. Therefore, the systems require Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) to convert signals between the analog and digital domains [1].

The mainstream ADC architectures are divided into Flash ADC, Successive Approximation Register ADC (SAR ADC), Pipeline ADC, Σ-Δ ADC and Hybrid ADC; and the mainstream DAC can be divided into R-2R ladder DAC, Current-steering DAC, Δ-Σ DAC, and Hybrid DAC. The basic working principles of ADCs and

DACs are illustrated in Figure 1 [2, 3]. As key modules in integrated circuit (IC) systems, ADCs and DACs facilitate the efficient conversion and application of analog and digital signals [4, 5].

Figure 1: The working process of the ADC and the DAC

High-performance ADCs and DACs are currently widely used in radar, communication systems, sensors, medical devices, and AI [4, 5]. However, achieving both high performance and low power consumption remains a major challenge in ADC/DAC design [6].

Existing studies mainly focus on unilateral optimization of ADCs/DACs' power consumption or performance, such as noise shaping. These efforts have mainly concentrated on NS-SAR ADCs and VCO-based ADCs, employing architectural optimization and tool innovations. However, systematic literature that reviews the development status of ADCs/DACs achieving both low power consumption and high performance remains limited.

This review aims to fill this gap by summarizing recent studies on low-power and high-performance ADCs and DACs. Through literature analysis and architectural comparison, it analyzes the current research status, identifies existing problems and limitations, and discusses potential optimization strategies to promote further development in this field.

The development of low-power and high-performance ADCs/DACs is essential for meeting the increasing demands of high-speed communication systems, intelligent sensing platforms, and portable medical devices. We have found that first-order NS-SAR ADCs offer a better trade-off between speed and power than second-order NS-SAR ADCs. Higher-order VCO-based ADCs achieve very low power but limited speed, while second-order VCO-based ADCs improve resolution and stability at higher power. The findings of this review are expected to provide useful insights for researchers in optimizing ADC/DAC architectures and developing more energy-efficient converters. Therefore, this work offers valuable guidance for future research on high-efficiency data converter design and contributes to the advancement of modern electronic systems.

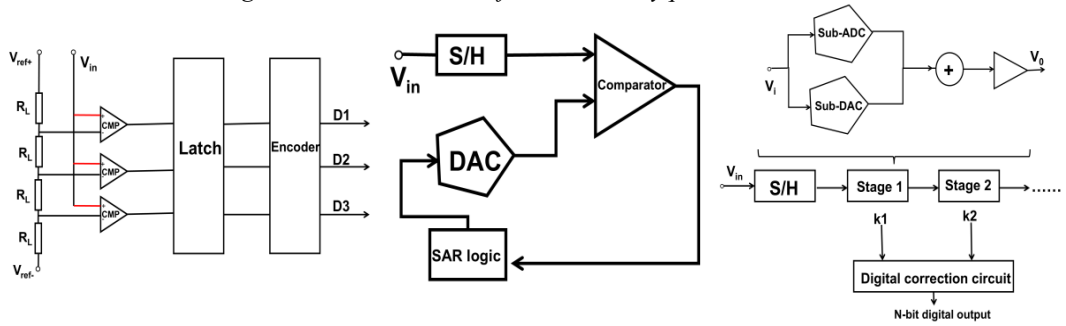
2. Literature Review

2.1 Performance Trade-offs of Mainstream ADCs/DACs

Different ADC architectures exhibit distinct trade-offs in speed, accuracy, and power consumption, and other aspects. Flash ADC offers fast calculation but consumes high power; SAR ADC realizes low power consumption with moderate speed and resolution; while Pipeline ADC offers a balance between speed and precision, though its multiple sub-stages lead to increased power consumption [2, 3, 5].

The above three ADCs are Nyquist-rate ADCs suitable for high-speed and low-precision scenarios [4]. Their structures are shown in Figure 2. In contrast, Σ-Δ ADC achieves high precision and high Signal-to-Noise and Distortion Ratio (SNDR) but typically operates at lower speeds [3-5].

Figure 2: The structures of traditional Nyquist ADCs in order



In terms of DAC architectures, the R-2R ladder DAC provides high precision and low power consumption but limited resolution; the current-steering DAC can accomplish high speed and wide bandwidth but exhibits significant static and dynamic errors; and the Δ-Σ DAC provides high precision and resolution but suffers from limited bandwidth and considerable delay [2, 5].

2.2 The Schreier Fom for ADCs and DACs

To analyze why low power consumption and high performance in ADCs/DACs are difficult to optimize simultaneously, we introduce the Schreier Figure of Merit (FoM) to examine this contradiction. A larger FoM indicates better performance at the same power consumption. For measuring the energy efficiency of ADC, we make use of the Schreier FoM, which was defined:

$$FoM=SNDR+10log_{10}\frac{BW}{P} \tag{1}$$

where SNDR is a method of ADC performance, BW represents the bandwidth, and P stands for power consumption [7]. From Eqution 1, for a constant FoM and bandwidth, higher SNDR indicates better performance which is accompanied by larger P.

Similarly, the Schreier FoM can be used to evaluate DAC efficiency, which is expressed as

$$FoM = SFDR + 10log_{10}\frac{BW}{P} \tag{2}$$

SFDR denotes Spurious-Free Dynamic Range, which is regarded as an approximate standard for DAC performance. For Eqution 2, higher SFDR means better performance and larger P. High-performance ADC/DAC inevitably correlates with high power consumption [9].

The Schreier FoM is prevalently used to measure the energy efficiency of ADC/DAC [7, 8]. Its formulation reveals a fundamental trade-off in ADC/DAC design: performance improvement is often accompanied by increased power consumption. Thus, achieving an optimal balance between performance and power consumption has become a key focus in ADC/DAC research. To address this challenge, researchers have explored various approaches, including the hybrid architectures, system optimization, and time- or frequency-domain ADC/DAC designs.

2.3 Hybrid Architectures and Performance Analysis

2.3.1 Recent Development of Hybrid Architecture

Existing ADC and DAC architectures have advantages and disadvantages, but neither can simultaneously be excellent in speed, resolution, and power consumption. In pursuit of low-power and high-performance ADC/DAC fabrication methods, researchers have focused on hybrid architecture. Given the performance constraints of conventional ADC/DAC architectures, hybrid architectures have been proposed and continuously developed [5]. Since the emergence of this concept, researchers have explored various hybrid architectures, including pipelined-SAR ADCs and segmented DACs [10].

Among various hybrid architectures, SAR-based ADCs have attracted considerable attention in recent years due to their favorable balance between power consumption, SNDR, and moderate resolution, but the SNDR related to resolution remains limited to 80 dB [11]. Resolution is influenced by factors such as noise and capacitor mismatch [12]. To address noise issues, researchers introduced NS techniques. From 2023 to 2025, noise-shaping (NS)-SAR ADCs have yielded notable research advancements, NS-SAR ADCs are examined in this study to analyze the development and limitations of hybrid architectures.

Nam et al. proposed a first-order NS-SAR ADC employing a PVT-insensitive closed-loop dynamic amplifier to improve noise suppression and system stability [13]. To further enhance noise-shaping capability, Cui et al. introduced a second-order NS-SAR architecture to reduces the high power consumption associated with conventional error-feedback (EF) schemes effectively [14]. Furthermore, Allam et al. proposed a novel architecture that shares conceptual similarities with time/frequency-domain ADCs [15]. They introduced an energy-efficient NS-SAR CDC architecture by modifying the NS-SAR ADC structure and substituting the input with a capacitor.

Despite these architectural improvements, capacitor mismatch remains a major factor limiting conversion accuracy. To address this issue, Xie et al. proposed a digital calibration method inspired by data-weighted averaging (DWA) to compensate for mismatch errors in SAR-based ADCs [12].

2.3.2 Function Analysis and Structural Limitations

The power consumption and performance data of the reported ADC designs are summarized in Table 1, where parameters not reported in the original references are denoted as "N/A".

Table 1: The power consumption and performance data for Hybrid ADCs

name	Xie et al. [12]	Nam et al. [13]	Cui et al. [14]	Allam et al. [15]
Process (nm)	55	28	65	130
Power Consumption (μW)	70	228	417	0.8
SNDR (dB)	66.9	71.2	78	74
FoMw (fs/conv·step)	7.9	9.6	N/A	2.05
FoMs (dB)	143.4	173.6	168	N/A
Fs (MS/s)	0.05	80	16	N/A
BW (MHz)	N/A	4	0.5	N/A

Different ADC architectures exhibit distinct power consumption and performance characteristics. Among the parameters listed in Table 1, Fs and BW mainly reflect the conversion speed, while the remaining indicators are closely related to the power efficiency of the converter.

The design reported by Allam et al. adopts a mature 130 nm process technology [15]. Benefiting from the relatively simple circuit structure, the power consumption is extremely low. However, the larger device size in this process node introduces higher parasitic capacitance, which limits the achievable circuit speed.

The works by Nam et al. and Cui et al. represent typical first-order and second-order noise-shaping SAR ADCs, respectively [13, 14]. The first-order noise-shaping SAR ADC can generally be implemented with a more advanced process node, resulting in lower parasitic capacitance and higher circuit operating speed, which leads to improved Fs and BW. In contrast, the second-order noise-shaping SAR ADC introduces additional integration loops and more complex control logic to enhance noise-shaping capability. The increased circuit complexity inevitably leads to higher power consumption, which is reflected by worse Power Consumption and FoM. Therefore, from the perspectives of power consumption and speed, the first-order NS-SAR ADC typically achieves lower energy consumption and higher conversion speed than the second-order structure, although the latter generally provides stronger noise suppression and higher accuracy.

Both Xie et al. and Nam et al. employ a first-order noise-shaping SAR architecture, but their optimization strategies are different [12, 13]. The former focuses on digital calibration techniques, while the latter mainly optimizes the analog circuit architecture. Digital calibration simplifies the analog circuitry and reduces power consumption, but it operates at a relatively low sampling rate. In contrast, analog circuit optimization enables significantly higher conversion speed at the cost of increased power consumption.

In summary, compared with the second-order NS-SAR ADC, the first-order NS-SAR ADC is generally more suitable for achieving a better trade-off between high conversion speed and low power consumption, although its noise suppression capability and accuracy are relatively limited. Furthermore, within the first-order NS-SAR architecture, different optimization strategies lead to different performance trade-offs. Digital calibration techniques typically favor lower power consumption but sacrifice conversion speed, whereas analog circuit architecture optimization tends to improve speed performance at the expense of higher power consumption.

2.4 Time/Frequency-Domain ADCs and DACs: Architectures and Performance Analysis

2.4.1 Recent Developments in Time/Frequency-Domain ADCs/DACs

Conventional and hybrid ADC/DAC architectures are primarily voltage-domain devices relying on high-precision operational amplifiers, leading to relatively high power consumption. Since digital circuits consume less power, researchers consider using time/frequency-domain ADCs/DACs to reduce power consumption. Typical examples include time-to-digital converter (TDC)-based ADCs, voltage-controlled oscillator (VCO)-

based ADCs, and pulse width modulation (PWM)-based DACs, which demonstrate improved power efficiency [6]. While PWM-ADCs/DACs have made slow progress in recent years , and they will not be discussed here.

A TDC processes input time intervals and can be integrated into the amplifier stage of an ADC to achieve high speed, low power, and high resolution. However, TDC still face challenges in time resolution and conversion accuracy. To address these issues, Y. Li et al. proposed a voltage–time hybrid architecture by introducing the voltage domain into a TDC-based ADC [17]. A split-TDC structure was employed to improve accuracy while maintaining low power consumption.

In contrast, the VCO is a circuit whose output oscillation frequency can be adjusted in response to the input voltage. Although VCO-based ADCs offer high digital compatibility, improvements are still needed in linearity and noise performance [6]. Loi et al. proposed a digital-to-frequency converter for dynamic power regulation, significantly improving resolution and bandwidth [16]. In addition, Kuo et al. reviewed second-order VCO-based ADC techniques and further proposed the concept of a third-order VCO-based ADC [6].

In contrast to the architectural innovations proposed by other investigators, Li et al. put forward the concept of an automated design generator named VSAGE in response to various demands [18]. As an end-to-end automated 16-bit ADC generator based on VCOs, VSAGE can automatically generate ADC designs starting from system-level specifications.

Beyond architectural innovations, Li et al. put forward the concept of an automated design generator named VSAGE in response to various demands [18]. As an end-to-end automated 16-bit ADC generator based on VCOs, VSAGE can automatically generate ADC designs starting from system-level specifications.

2.4.2 Function Analysis and Structural Limitations

Research in the time/frequency domain primarily focuses on TDC-based ADC, while VCO-ADC also attracts attention. The data of various time/frequency-domain ADCs and DACs are summarized in Table 2, and some parameters are marked as “N/A” because they were not reported in the original references.

Table 2: The data of time/frequency-domain ADCs/DACs

name	Kuo et al. [6]	Loi et al. [16]	Li et al. [18]		Li et al. [17]
Process (nm)	65	130	28	65	28
Power Consumption (μW)	4.4	105.6	494	885	7930
BW (MHz）	0.0025	0.02	3	2.5	N/A
SFDR (dB)	119.6-123	N/A	N/A	N/A	72.16
FOM_S (dB)	179.6	155.5	172.4	165.6	N/A
Area (mm^2)	0.1	0.022	0.016	0.028	0.033
SNDR (dB)	92.1	N/A	74.61	71.1	65.66

The works by Kuo et al. and Loi et al. represent higher-order VCO-based ADC and second-order VCO-based ADC architectures, respectively [6, 16]. The higher-order VCO-based ADC achieves extremely lower power consumption of 4.4μW and a higher FoMs [6]. However, its bandwidth is extremely small, indicating a very limited conversion speed. In contrast, the second-order VCO-based ADC proposed adopts a digital pseudo-DCO structure, which improves system stability and resolution [16]. Nevertheless, the additional control circuitry leads to significantly increased power consumption. This comparison indicates that in VCO-based ADCs, more complex control structures can improve performance robustness but usually introduce additional power and area overhead.

Compared with the circuit-level optimizations, the work by Li et al. focuses on the design methodology rather than proposing a new VCO-based ADC circuit structure [6, 16, 18]. Specifically, the authors introduced VSAGE, an automated design generator capable of producing Δ-Σ ADC architectures based on VCO from system-level specifications. This approach significantly improves design efficiency and scalability. The generated architecture achieves a better balance among speed, resolution, and power consumption. Although the power consumption increases to 494μW, the bandwidth is significantly extended to 3 MHz while maintaining an SNDR of 74.61 dB and a FoMs of 172.4 dB [18].

Different from the frequency-domain VCO-based ADCs, Li et al. adopted a voltage–time hybrid-domain architecture combined with a Time-to-Digital Converter (TDC) to achieve high-speed quantizationin [6, 16, 18]. By employing time encoding and high-speed TDC-based conversion, the proposed design significantly

improves conversion speed and bandwidth. However, to enhance time resolution and accuracy, a split-TDC structure is introduced, which increases the circuit complexity and results in substantially higher power consumption of approximately 7.93 mW compared with the VCO-based ADC designs.

In summary, different architectures exhibit distinct advantages as well as inherent limitations. The higher-order VCO-based ADC achieves extremely low power consumption and high energy efficiency, but its conversion speed is limited. The second-order VCO-based ADC improves system stability and resolution, yet this improvement comes at the cost of increased circuit complexity and higher power consumption. The VCO-based ΔΣ ADC generated by VSAGE and the voltage–time hybrid ADC with TDC-based quantization provide new design perspectives. However, they still cannot overcome the inherent trade-off among speed, resolution, and power consumption.

3. Future Prospects of ADCs/DACs

Despite significant progress in hybrid architectures and time/frequency-domain techniques, neither conventional ADC/DAC architectures nor hybrid, time/frequency-encoded designs can fully resolve the inherent trade-off. Achieving an optimal balance between these two metrics remains a critical challenge and an active area of research.

According to current research, I infer that NS-SAR ADC represents the most promising option for low-power and high-performance hybrid architectures. In recent years, the NS-SAR ADC has consistently been featured in journal publications with updated FoM [11, 13, 14, 15]. Its scalable digital path provides a multi-dimensional scope for subsequent enhancements, and its high compatibility injects significant potential for future commercialization. Regarding time/frequency-domain ADC/DAC, the TDC-based ADC represents the most extensively researched and promising direction. Its multi-channel or hybrid architecture optimization capabilities give it greater room for performance enhancements and make it more likely to achieve a compromise between low power consumption and high performance.

4. Conclusions

In recent years, significant progress has been made in the development of ADCs and DACs, particularly in hybrid architectures and time/frequency-domain designs. This paper systematically reviewed existing research, highlighting both the achievements and the ongoing challenges in this field. It was found that first-order NS-SAR ADCs provide a better trade-off between high conversion speed and low power consumption compared with second-order NS-SAR ADCs.

And higher-order VCO-based ADCs achieve extremely low power consumption and high energy efficiency but limited speed. Second-order VCO-based ADCs improve stability and resolution at the cost of higher power consumption and complexity. Novel design methods, such as VSAGE, provide new perspectives but still cannot fully overcome the inherent trade-offs.

However, this paper has not yet reviewed the research progress on developing novel ADC/DAC architectures, and future articles may focus on the analysis of specific structures and accuracy-related issues. With technological advancements, it is anticipated that next-generation ADCs/DACs with lower power consumption and higher performance will emerge, which could be NS-SAR ADCs or entirely new architectures. These devices will further inject greater momentum into areas like communication systems, sensors, and other technologies, contributing to the realization of more advanced and convenient lifestyles.

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Funding

This research received no external funding.

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgment

This paper is an output of the science project.