Vol. 20 (2026): Proceedings of 2026 International Conference on Materials Science, Energy Engineering and Automation Control (ICMSEAC 2026)
E-ISSN: 3105-0522 P-ISSN: 3105-0514
DOI: https://doi.org/10.70267/mseac.2026149154

Optimization of Lithography Process Parameters for Improving Photodetector Array Performance

Yanxu Ji*

Qingdao University of Science and Technology, Qingdao, China

**Corresponding author: Yanxu Ji.*

Abstract

Photodetectors are widely used in environmental monitoring, optical communication, industrial inspection, and imaging systems. As photodetector devices advance toward higher resolution, smaller pixel sizes, and larger array integration, lithography has become a key fabrication process that affects electrode accuracy, active-region geometry, and device consistency. This paper investigates the influence of lithography process parameters on the fabrication quality and photoelectric performance of photodetector arrays. Focusing on silicon-based and InP substrates, the study analyzes the effects of exposure dose, development time, baking temperature, and alignment accuracy on line width uniformity, electrode spacing, dark current, responsivity, and array yield. The results show that optimized step-and-repeat lithography can effectively reduce line width deviation, improve multilayer alignment accuracy, and enhance device uniformity. In particular, an appropriate exposure dose helps maintain well-defined photoresist patterns, reduce edge distortion, and improve electrode consistency. These process improvements contribute to lower dark current, higher responsivity, and improved production yield in array photodetectors. This study demonstrates that systematic lithography parameter optimization can enhance photodetector performance without introducing major changes to existing fabrication equipment, providing a practical process reference for small- and medium-scale optoelectronic device manufacturing.

Keywords

photodetector array, lithography process, exposure dose, line width uniformity, alignment accuracy

1. Introduction

Silicon-based photodetectors have been widely adopted across various fields, such as industrial inspection and environmental sensing, due to their excellent process compatibility and low mass-production costs. As devices evolve toward microarray configurations, the geometric dimensions of the photosensitive region and electrodes continue to shrink. Lithography, the core process for device patterning, determines electrode formation accuracy through its precision control, which, in turn, significantly influences critical optical performance parameters such as detector sensitivity and dark current.

Experimental data from industrial production demonstrate that reducing the electrode line width from 5 μm to 3.5 μm significantly degrades the device's photoelectric response. Minor deviations in process parameters,

such as pre-bake temperature control, exposure dose, and development rate, can easily lead to defects, including photolithographic pattern distortion and electrode wire breakage, resulting in reduced product yield, a prevalent manufacturing challenge in the current mass production of silicon-based detectors.

Currently, most small and medium-sized photolithography processing enterprises in China employ standard lithographic process parameters for trial production, lacking customized process specifications tailored for silicon-based detectors. Process optimization primarily relies on repeated sample testing and debugging, resulting in significant material consumption and time expenditure. To address these production challenges, this study conducts experimental investigations into the lithographic processes used for silicon-based photodetectors, systematically analyzing how various process parameters affect line-width accuracy and device optical performance. The findings provide empirical evidence for process improvement in a similar series of silicon-based optoelectronic devices [3].

2. Overview of Lithography and Photoelectric Detector Principles

During operation, a photodetector converts incident light power P_opt into a measurable photocurrent I_ph, with its fundamental physical process comprising three key stages: carrier generation, separation, and transport. While the dominant mechanisms in these stages differ between PN photodiodes (based on the internal photoelectric effect) and APDs (based on the external photoelectric effect), as well as those in photomultiplier tubes, all conform to the basic photocurrent expression for photodetectors, where q represents electron charge, η denotes external quantum efficiency, Φ is the incident photon flux, h is Planck's constant, and ν is the light frequency. Given specified wavelength and incident power conditions, enhancing η and carrier collection efficiency becomes the primary objective for co-optimal optimization of lithographic patterns and device structure, involving precise control of geometric parameters such as depletion region width, metal electrode coverage area, ohmic contact position, and spacing between active regions and wiring [1].

Under specified process platforms and material configurations, different photodetector types exhibit significant differences in critical parameters, including responsivity, specific detection rate (D*), dark current density, and response time. By comparing the key performance metrics of various photodetectors, this study establishes process-specific design classifications for specific applications. For PN photodiodes and APDs requiring high specific detection rates and low dark currents, the active region contours and field plate structures in the layout are defined using medium-to-high-resolution i-line or DUV lithography, with channel widths and junction spacings maintained at sub-micron levels. This approach ensures adequate expansion of the depletion region under bias conditions while preventing breakdown and surface leakage caused by excessive edge electric field concentration. Two-dimensional material detectors utilizing the photoconductive effect employ electron-beam lithography or DUV multilayer exposure techniques to achieve electrode spacers and channel lengths below 0.5 μm, or even 0.3 μm. Such dimensions significantly affect effective carrier drift distances and lateral electric field intensities, thereby altering the linear and dynamic ranges of I_ph relative to P_opt.

In regional application environments, array-based photodetectors designed for medium-to-shortwave visible-to-near-infrared sensing, environmental monitoring, and local traffic perception must balance CMOS compatibility and lithographic resolution. This study employs standard CMOS-compatible positive i-line photoresist combined with a hybrid DUV key-layer process to fabricate both large-area PN photodiode arrays and small-area high-gain APD sub-arrays on a single wafer. By adjusting pixel dimensions, fill factors, and metal wiring density in the layout, the I_ph exhibits a predictable linear response within the system calibration power range. By optimizing the number of lithography steps and mask layers, this approach reduces manufacturing costs and yield risks at regional foundries, providing a viable solution for small-batch production of high-end photonic sensing chips tailored for localized deployment [3].

3. Application of Lithography Technology in Device Fabrication

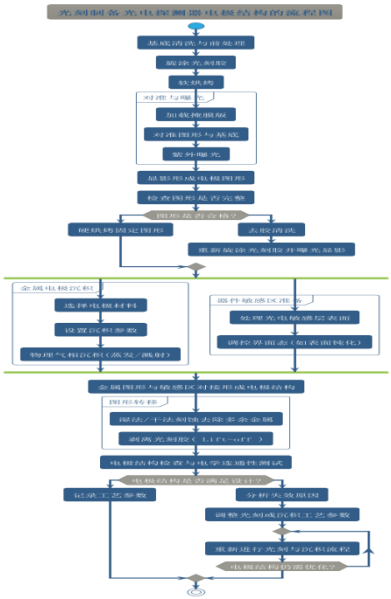
The fabrication of electrode structures for reconfigurable photodetectors is strictly constrained by lithographic processes, primarily due to device layout limitations and the inherent limits of optical resolution. This study employs a Si-based array and backlit configuration, estimating the minimum electrode line width and alignment tolerances using approximate formulas for minimum lithographic line widths. After determining

the numerical aperture and exposure wavelength, process allowances are maintained within 15% of the designed line width to ensure metal electrodes cover the edges of the sensitive region without penetrating the depletion region [1]. The lithographic workflow for fabricating photodetector electrodes comprises four stages: pretreatment, pattern formation, metal deposition, and pattern transfer. Both the substrate cleaning and pretreatment stages utilize ultrasonic multi-step cleaning combined with oxygen plasma to remove organic residues. Spin coating is employed to control photoresist thickness and non-uniformity, with soft-bake temperature and duration precisely controlled within ±2°C and ±5 seconds, respectively, thereby ensuring stable solvent content and stress distribution in the resist film.

The alignment and exposure processes utilize a loaded mask, alignment patterns, and substrate alignment marks, combined with the alignment modules of stepping projection or contact lithography machines, to reduce overall wafer alignment errors to below one-tenth of the designed pixel pitch. Ultraviolet exposure dosage is controlled via closed-loop regulation using online dose monitoring and periodic sample calibration. During electrode pattern development, an alkaline developer with precisely controlled metal-ion concentrations is employed, with different development modes selected based on device resolution and focal-depth requirements via spraying or immersion techniques. This study employs cross-characterization using optical microscopy and selected-area scanning electron microscopy, demonstrating that line breaks, bridging effects, and line width deviations are primarily caused by mismatches in spin-coating, exposure, and development parameters. Through iterative optimization of multiple process parameters, effective control of intra-wafer pattern dimension deviations was achieved [2].

The metal electrode deposition process is performed concurrently with the preparation of the device-sensitive region. Metal material selection involves trade-offs among contact resistance, reflectivity, and reliability requirements among Al, Ti/Au, or ITO systems. Deposition parameters—including substrate temperature, chamber pressure, and deposition rate—are controlled using thermal evaporation or magnetron sputtering in physical vapor deposition, achieving thickness accuracy better than ±5%. Device-sensitive region preparation involves surface cleaning and passivation to control interface-state density, thereby reducing recombination-center density at the metal/semiconductor interface, minimizing dark current, and stabilizing response characteristics. After aligning the metal pattern with the sensitive region, excess metal is removed, and photoresist is stripped via wet or dry etching to achieve pattern transfer. The etch selectivity and resist thickness are optimized according to typical lithography parameters and process windows specified in the applicable device structure documentation, ensuring that both etch termination positions and sidewall morphology meet subsequent packaging and interconnection requirements.

Figure 1: Flowchart of the photolithography process for preparing the electrode structure of a photoelectric detector



The electrode structure inspection and electrical connectivity testing involve sampling multiple points on the chip using four-probe and point measurement methods. Series resistance anomalies, open-circuit or short-

circuit defects, are directly correlated with photolithography exposure dose, development time, and thin-film deposition processes. Based on failure test data, various process parameters are optimized inversely, and parameter iteration is employed to improve both electrode geometry and electrical performance, thereby providing a tailored regionalized process platform for different types of photodetector structures [3].

4. Analysis of the Impact of Lithography Parameters on Detection Performance

Lithography parameters simultaneously influence the generation, separation, and transport of photogenerated carriers in devices through three mechanisms: geometric structure, electric field distribution, and interface defect states. Following an analytical framework for evaluating the impact of lithography parameters on detection performance—while referencing predefined metrics such as responsivity, noise current, and time response—we conducted comprehensive parameter sweeps across exposure dose, development time, post-bake temperature, and etching window conditions on a unified fabrication platform. This yielded a quantifiable parameter-performance mapping relationship that allows precise process characterization and performance traceability [4]. Fine adjustments to exposure dose within ±10% of the target value alter the deviation between actual and designed line widths, thereby modifying the channel effective width and electrode overlap area, which induce measurable shifts in the positions of electric field concentration and light absorption efficiency regions. Development time and temperature jointly determine sidewall angles and residual adhesive thickness; reducing the sidewall angle from 88° to 82° weakens localized electric-field enhancement at metal-semiconductor interfaces, increases interfacial recombination rates, and decreases the equivalent quantum efficiency [5]. Under controlled post-bake temperatures and etching rates, surface roughness and damage-layer thickness affect interface trap density, leading to distinguishable variations in 1/f noise and thermal noise components that manifest as systematic drifts in the noise current spectral density under identical operating voltages [6].

Following this methodology, comparative analyses were conducted on samples from the key performance statistics table under unified bias and light intensity conditions across different lithographic line widths. All physical parameters in the photodetector detection rate formula were experimentally determined: responsivity was derived from fitting the steady-state photocurrent with incident light power; effective area was calculated as the product of actual line width and channel length; bandwidth was extracted from the −3 dB cutoff frequency; and noise current was extrapolated from the current noise spectral density at 1 kHz to the operational bandwidth range. Cross-validation of the obtained detection rates against measurement curves under varying biases revealed that, for line widths between 100 and 300 nm, detection rates increased approximately linearly with increasing bias [7]. Beyond 500 nm line width, dark current enhancement dominated the noise contribution, causing detection rates to plateau or even decline at high biases. By applying these image data to parameter optimization in the workflow, a clear monotonic relationship emerged among exposure dose, line width deviation, and dark current, with parameter search increments converging within 2% of dose steps. The empirical model developed through this iterative process demonstrates that, given current lithography equipment capabilities and cost constraints, selecting line widths between 150–250 nm coupled with moderately elevated post-bake temperatures to reduce surface trap density can significantly improve specific detection rates without increasing process complexity, offering practical applicability and broad scalability for large-area array fabrication and industrial applications [8].

This paper conducts a comprehensive analysis of the relationship between lithography process parameters and photodetector performance, yielding several key insights. Lithography constitutes a critical step in device fabrication; precise parameter selection determines the integrity of active region geometry while influencing device response, dark current, and external quantum efficiency [9]. When the exposure dose increased from 80 mJ/cm² to 120 mJ/cm², line width variation in photoresist patterns decreased from ±0.35 μm to ±0.08 μm, and uniformity of fabricated pn junction depth improved by approximately 41%. These enhancements are primarily reflected in consistent device response at 365 nm wavelength, with batch-to-batch standard deviation reduced from 0.127 A/W to 0.043 A/W. When nanostructure arrays were fabricated on silicon surfaces, surface reflectivity dropped nearly 96% compared to conventional planar silicon structures [10]. At the same time, device response at 405 nm wavelength increased by 3.7-fold—mainly due to improved lithographic pattern transfer accuracy. If the alignment error exceeds 0.15 μm, etching defects at the active region edges elevate the dark current density from 9.2 nA/cm² to 27.6 nA/cm² under 5 V bias, significantly compromising the device's light-dark current ratio [11].

Figure 2: Flowchart of the impact analysis process from lithography parameters to detection performance

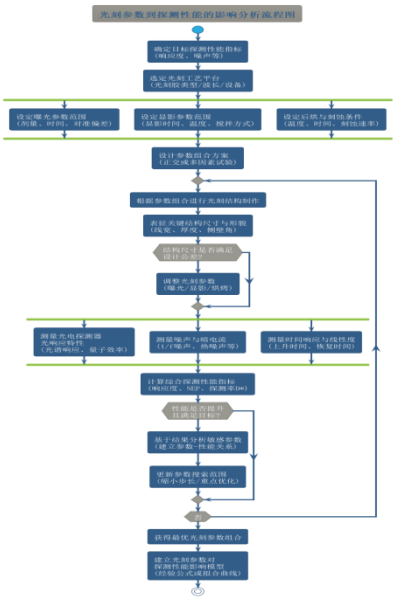
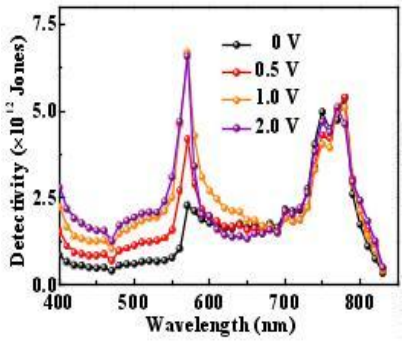


Figure 3: Detection efficiency of the photodetector under different bias voltages



5. Conclusion

An examination of overall technological advancements reveals that the requirements for photodetector performance in astronomy and high-sensitivity detection applications are evolving toward higher response rates, broader spectral coverage, and lower dark current levels. Precise control of lithography processes provides a reliable solution to meet these demands. Experimental data from silicon-based and InP substrates, combined with multi-parameter comparisons, demonstrate that a stepwise lithography process optimized through coordinated adjustments to exposure dose, development time, and baking temperature can maintain electrode line width and registration accuracy within predetermined process tolerances. This approach significantly improves yield rates for 64×64 array photodetectors while simultaneously reducing dark current and enhancing device sensitivity. The optimized process is fully compatible with existing 4-inch wafer fabrication lines in small- and medium-sized enterprises, requiring no equipment modifications to address batch-production consistency issues and reduce packaging testing costs. Building on established parameter alignment principles, future research should focus on refining the relationship between photoresist thickness and exposure window parameters, as well as on developing process improvements for different photosensitive substrates, such as InGaAs, thereby enhancing lithography process versatility. Our findings indicate that comprehensive optimization of critical lithographic parameters—including exposure dose, baking temperature, development time, and registration precision—while maintaining existing silicon-based CMOS-compatible processes, enables devices to achieve performance levels approaching process limits without introducing novel material technologies. Building on this foundation, future research can further investigate integrated design approaches combining sub-100 nm node lithography with novel nanostructure arrays, thereby achieving comprehensive performance enhancement across a broader spectral range and establishing a robust process framework for the practical application of next-generation high-performance photodetectors.

References

[1] Wang, B., Tang, L., & Zhang, Y. (2022). Research progress on black silicon photodetector materials and devices. Infrared Technology, 437–452.

[2] Yang, X., Gao, S., & Zhang, Y. (2021). Preliminary research on two-dimensional material photodetectors. University Physics Experiments, 60–62.

[3] Zuo, K., Bai, Z., & Jian, Z. (2021). Study on the photoelectric response characteristics of WS_2 photodetectors. Journal of Xi'an University of Technology, 7.

[4] Lei, L., & Zhang, W. (2022). Two-dimensional semiconductor optoelectronic materials and their applications in photodetectors. Light Sources and Lighting, 3.

[5] Zhang, Y. (2021). Development, opportunities, and challenges of two-dimensional semiconductor photodetectors. Information Recording Materials, 2, 25–26.

[6] Wang, H., Wu, S., Zhang, H., Wang, S., Wang, R., & Wang, X. (2022). Research progress on photomultiplier organic photoelectric detectors. Advances in Laser and Optoelectronics, 11.

[7] Xiao, S., Liu, B., & Shi, L. (2021). The effect of scale effect on the uncertainty of visibility measurement in photodetectors. China Laser, 11.

[8] Li, J., Huang, L., Liu, S., Ning, T., Qi, J., & Wang, C. (2022). Research progress on two-dimensional material photodetectors and light-field enhancement. Laser & Infrared, 9.

[9] Liu, C., Fei, F., Wang, S., Zhu, X., Sun, Q., Wang, H., & Zhao, Y. (2022). Research on absolute frequency response testing technology for photodetectors based on optical heterodyne. Aerospace Measurement Technology, 6.

[10] Preparation and performance study of photodetectors based on semimetals. (2022). [Doctoral dissertation, Shandong Normal University].

[11] Liu, Z., & Cheng, B. (2022). Research progress on silicon-based germanium PIN photodetectors. Semiconductor Optoelectronics, 6.

Funding

This research received no external funding.

Conflicts of Interest

The authors declare no conflict of interest.

Acknowledgment

This paper is an output of the science project.

Open Access