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Application Prospects and Challenges of Micro-Nano Memristors

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Abstract

This paper reviews the basic structure, material systems, operating principles, and application progress of memristors. First, the typical metal-insulator-metal (MIM) structure of memristors is introduced, along with the characteristics of various insulator materials such as metal oxides, two-dimensional materials, and phase-change materials. Subsequently, research progress in simulating biological synapses, achieving physically non-clonable functions, and enhancing data processing efficiency is outlined across various domains including neuromorphic computing, hardware security, data preprocessing, and multi-level storage. Despite advantages in storage density and computational approach, resistive memory devices currently face challenges such as unstable resistance states and inherent device-to-device variations, limiting their readiness for large-scale practical deployment. Recent efforts in material doping and interface engineering have yielded improvements in device uniformity and stability. However, further optimization of material systems and device structures remains essential to enhance reliability and controllability for future applications.

Keywords

nanoscale memristors, neuromorphic computing, hardware security, machine learning

1. Introduction

A memristor is a nonlinear resistor capable of storing the amount of charge that has passed through it. It is a device that represents the relationship between magnetic flux and charge. Essentially, a memristor is a memory resistor with a MIM (metal-insulator-metal) structure, featuring an insulating layer material sandwiched between two metal electrodes. The basic structure of the memristor is shown in Figure 1.The insulating layer in the middle possesses unique properties: it undergoes reversible changes in resistance under the influence of an applied physical field, and this resistance state persists even after the external field is removed, thereby achieving memory. The resistance can transition from a low-resistance state to a high-resistance state and vice versa, earning it the name “resistance switch.” Since memristors can store the high-resistance state (0) and the low-resistance state (1), they can be used for information storage. Based on the resistive change mechanism of the intermediate insulating layer material, memristors primarily include metal oxide-type, phase-change-type, perovskite oxide-type, organic polymer-type, solid-state electrolyte-type, two-dimensional-type, elemental-type, and others. Currently, the most common insulating layer material in memristors is binary oxides. A large number of binary oxides have been found to exhibit memristive properties, primarily transition metal oxides, lanthanide oxides, and some non-metallic oxides [1]. The most representative type is the metal oxide memristor, whose basic structure is shown in Figure 2. Additionally, phase-change memristors are another common type, with their basic structure shown in Figure 3.

Figure 1: Schematic diagram of the basic structure of a memristor

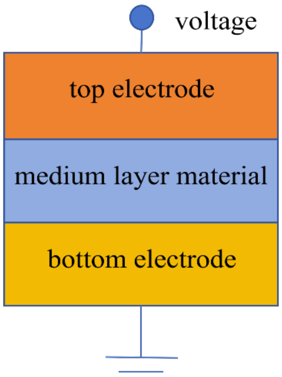


Figure 2: Schematic diagram of the metal oxide memristor structure. (a) Low-resistance state after growth of conductive filaments in the oxide layer; (b) High-resistance state after breakage of conductive filaments in the oxide layer

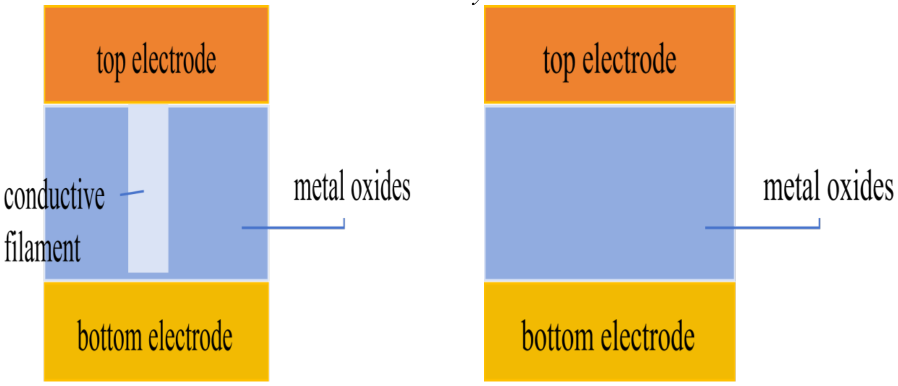
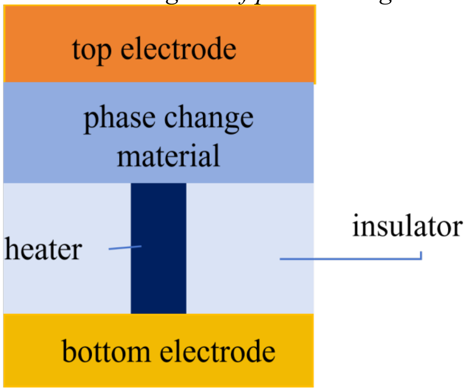


Figure 3: Schematic diagram of phase-change memristor structure



Since memristors can inherently store two distinct resistance states, they serve as natural information storage units. After applying an input pulse voltage, resistance state information is stored. Subsequently, by measuring the current value after applying a small read voltage, the stored resistance state information can be retrieved. This read process is essentially a computational operation. Unlike traditional computers, which require data to be read from memory (DRAM) into the processor's (CPU) registers, computed, and then written back to memory, memristors inherently achieve storage and computation in a single unit. This capability breaks through the von Neumann bottleneck.

Due to the simple fundamental structure of memristors and the fact that the basic functional unit dimensions required for their resistive switching mechanism are inherently nanoscale, current memristor materials can already achieve nanoscale dimensions. Table 1 lists common types of memristors along with their corresponding electrode materials and insulating layer materials. The three-layer fundamental structure of memristors can be realized with extremely thin dimensions through thin-film deposition techniques. The intermediate insulating layer can be controlled to a thickness of several nanometers using thinning techniques, such as the ultra-thin antimony film and ultra-thin GeTe layer in phase-change memristors [2]. For two-dimensional memristors, graphene is commonly used as the intermediate functional layer, as graphene [3] itself is an atomically thin two-dimensional material. Additionally, materials for elemental memristors, such as amorphous silicon and amorphous carbon [1], can also be fabricated at the nanoscale. For the most common metal oxide memristors, their resistive switching mechanism relies on the growth of conductive filaments within the oxide layer to achieve a high-resistance state, as shown in Figure 2(a), and the breakage of these filaments to achieve a low-resistance state, as shown in Figure 2(b). The conductive filaments themselves are nanowires. This can be achieved through techniques such as UV lithography and 3D integration.

Table 1: Common types of memristors and their corresponding materials

Type	Insulation layer material	Electrode materials
Metal oxide	ZrO_2	Ta TiN
Metal oxide	Al_2O_3	Cu Pt
Metal oxide	HfO_2	Ta Pt
Metal oxide	ZnO	Ag Pt
Metal oxide	Bi SnO_2	ITO TiN
Metal oxide	SiO_2 Ag	Au Ti
Metal oxide	TaO_X Ta_2O_5	Pd Pd
Metal oxide	TiO_X TaO_Y	Ti Pt
Metal oxide	HfO_2 TiO_X	Ti Pt
Phase-change	Sb_2Te_3	TiN TiN
Phase-change	$Ge_2Sb_2Te_5$	TiN W
Phase-change	GeTe	TiN Ti
Two-dimensional material	PTCDA h-BN	MoS_2 WSe_2

As memristors achieve nanoscale dimensions in material size, their application scenarios have also evolved, expanding into broader fields. The nanoscale dimensions not only enhance information storage density but also create the necessary conditions for realizing compute-in-memory computing. Consequently, they can be applied in high-end technology industries such as neuromorphic computing, device security and key generation.

2. Application Areas

2.1 Applications in the Field of Neuromorphic Computing

Due to their nanoscale dimensions, memristors can simulate biological synapses, making them applicable to neuromorphic computing. In biological neurons, synapses alter their transmission capacity by releasing Ca^{2+} ions in response to external stimuli, thereby transmitting pulse signals between neurons for information processing. The resistance value of a memristor depends on its past state, functioning similarly to neural synapses and enabling simulation of the brain's information processing mechanisms. Researchers have successfully achieved key synaptic functions using various material systems—such as TiO_X, HfO_X, TaO_X, ZnO_X, and organic compounds—as insulating layers in memristor fabrication. These include: triggering excitatory postsynaptic currents (EPSCs) with optical pulse assistance; simulating learning-forgetting-relearning processes via memristor arrays; and realizing long-term potentiation (LTP), long-term depression (LTD), and paired-pulse facilitation (PPF) [4]. Only by scaling memristors to the nanoscale can millions or even billions be integrated onto a single chip, achieving synaptic densities comparable to biological systems. This makes the formation of large-scale crossbar arrays possible, enabling complex neural network models. Moreover, nanoscale devices typically operate at lower voltages and currents, which is crucial for reducing the total power consumption of large-scale parallel computing. This makes their energy efficiency far surpass traditional technologies, enabling them to meet demanding scenarios like edge computing. Compared to CMOS-based neuromorphic networks, RRAM arrays—a typical memristor implementation—achieve over 1000 times faster processing speeds while reducing power consumption by four orders of magnitude [5].

2.2 Applications in the Field of Hardware Security

With the advent of the information age, security concerns have become increasingly prominent and worthy of attention, with hardware security being of paramount importance. The high-resistance and low-resistance state switching of RRAM memristors relies on the random formation and breakage of internal conductive filaments. This process occurs at the atomic scale and is influenced by random factors such as thermal effects and ion random migration. Even for the same memristor, the speed of its resistance state switching will exhibit subtle and unpredictable fluctuations across multiple cycles. This inherent randomness means we cannot precisely predict or control the exact behavior of a single RRAM at a specific voltage. This also forms the physical basis for generating random numbers used for keys. Moreover, due to the limitations of manufacturing processes, even two memristors with identical designs on the same chip exhibit inherent nanoscale variations in parameters such as the thickness of the dielectric layer and the roughness of the electrodes [6]. These variations cause differences in initial resistance, formation voltage, and resistance state switching characteristics, endowing each resistive memory array with a unique “resistance pattern.” In the field of hardware security, the instability of memristors—such as their resistance drift—actually holds greater significance, differing from the storage domain where stable parameters are required. When fabricating an array composed of numerous memristors on a chip, a Physically Unclonable Function (PUF) can be realized. When a small, identical read voltage is applied to each memristor in the array, their inherent, irrepressible differences cause them to exhibit distinct responses: some maintain the high-resistance state (0), while others remain in the low-resistance state (1). The binary string representing the entire array's response pattern recorded at this point constitutes the chip's unique key. When verifying device identity—such as when IoT devices access cloud servers—the system transmits the same read signal again. The memristor array on the chip then generates a corresponding response pattern. The system compares this newly generated response with the previously stored initial response. If they match, access is granted; if they differ, access is denied. Since each chip's PUF response is unique, cloning a device is virtually impossible both economically and technologically. Traditional methods store keys in memory, making them vulnerable to detection and theft. In contrast, PUF keys are essentially generated on-demand and leave no trace on the chip after use, significantly enhancing key confidentiality. Zhang et al. constructed a nanoscale $Ag:SiO_2$ diffusion-type memristor cross array to implement the PUF [7]. This PUF leverages the random distribution of Ag ion clusters within the SiO_2 substrate, converting it into a random binary bitmap that serves as the device fingerprint. This approach achieves highly random and uniquely identifiable PUF responses.

2.3 Other Applications

Beyond neuromorphic computing and hardware security, memristors also find extensive applications in other fields. Many machine learning algorithms typically require data preprocessing to classify datasets, a function that metal oxide memristors can perform exceptionally well. Choi et al. [8] constructed a cross-array structure using a dual-layer memristor based on $Pd/TaO_X/Ta_2O_5/Pd$. This structure enables online, unsupervised principal component analysis (PCA) on raw static data, physically reducing the dimensionality of high-dimensional data while extracting key features. By performing preprocessing and feature extraction before data computation, it enhances the efficiency of subsequent operations. Meanwhile, Zhong et al. [9] developed a $Ti/TiO_X/TaO_Y/Pt$ dual-layer memristor capable of speech recognition, achieving a speech recognition error rate of only 0.4%. This demonstrates that oxide-based memristors can also perform precise preprocessing on dynamic data that changes over time. Compared to single-layer memristors, dual-layer memristors exhibit more stable switching parameters, not only improving classification efficiency but also reducing the workload of peripheral circuit design. For high-density large-scale data, nanoscale memristors inherently facilitate high-density storage. Ismail et al. [10] achieved precise control over the reset cutoff voltage by inserting an amorphous zinc-tin oxide (a-ZTO) interface layer within the ZrO_2 medium layer. This enabled the realization of one distinct low-resistance state and three high-resistance states within a single device. This breakthrough enables dual-layer memristors to overcome the physical limitations of traditional binary storage. By implementing multi-level storage, they achieve a significant increase in data storage density per unit area, providing a practical device foundation for constructing high-capacity non-volatile memory.

3. Current Situation and Challenges

As a memory device, a memristor should ideally retain its resistance value after power loss to achieve non-volatile data storage. This constitutes the core function of a memristor—its “memory”. Furthermore, memristors require high stability, rapid resistance change rates, extended operational lifespans, and superior durability.

The performance of current memristor materials at the nanoscale has not yet reached an ideal state. Structural relaxation in the amorphous phase causes resistance drift over time [2], significantly degrading multi-value storage accuracy. Furthermore, most memristors fail to meet ideal standards for multiple properties, including conductance linearity, periodic behavior, device-to-device consistency, and power consumption [3].

3.1 Stability Issues

The most critical issue is the stability of memristors. Memristors often exhibit structural resistance distribution irregularities or resistance drift, which can lead to erroneous read and write operations or even device failure. This stems from the core physical mechanism of memristors. Whether based on the relatively rapid resistive switching driven by conductive filament growth or the slower resistive switching mediated by interface modulation, both fundamentally rely on the migration and redistribution of ions or defects at the nanoscale or even atomic scale. This microscopic process exhibits inherent randomness and thermodynamic instability. Addressing the stability issue of memristors is a prerequisite for achieving high-reliability, high-precision information storage and computation.

Within the same array, parameters of different memristor units—such as set voltage, reset voltage, and high/low resistance values—often exhibit significant dispersion. For typical metal-oxide memristors, instability primarily manifests in the random growth of conductive filaments. For instance, the resistive switching in $Ta/HfO_2/Pt$ structures is dominated by localized conductive filaments connecting electrodes. In 2016, Jiang et al. employed scanning transmission electron microscopy (STEM) and electron energy loss spectroscopy (EELS) to physically characterize $Ta/HfO_2/Pt$ devices [11], directly observing a sub-10-nanometer conical conductive channel enriched in Ta and depleted in oxygen. This demonstrated migration of the active electrode Ta, refuting the notion that the resistive switching mechanism in HfO_2 devices is solely governed by oxygen ion motion. The conductive channel was identified as an amorphous Ta-O solid solution [11] rather than a pure metallic filament. The formation process of this structure is highly dependent on the initial defect distribution, local electric fields, and thermal effects, inherently exhibiting randomness. Across different devices, the nucleation sites, pathways, and final morphologies of filaments are difficult to reproduce, which directly causes parameter dispersion among memristor units. Such non-uniformity leads to inaccuracies in memristor information recognition. In neuromorphic computing applications, the conductance value of a memristor represents synaptic weight. Precise, linear weight modulation is fundamental to efficient learning. However, memristors in traditional single-material systems often exhibit nonlinear and asymmetric conductance values. In their study on flexible TiO_2-WO_{3-X} hybrid memristors, Pan et al. demonstrated the impact of material homogeneity by quantifying nonlinearity factors and asymmetric nonlinearity factors. Undoped WO_{3-X} devices exhibited strong nonlinearity and poor symmetry in conductance variation [12]. This non-uniformity implies that identical electrical pulse stimuli produce vastly different conductance changes across different devices or during different cycles within the same device.

When constructing convolutional neural networks for handwritten digit recognition, the maximum recognition accuracy achieved was only 93.4% [12]. Furthermore, performance deteriorates sharply as the precision requirements for device control increase. In other words, resistive non-uniformity directly compromises the computational accuracy of neuromorphic systems.

Furthermore, in conductive filament-type memristors, the conductive filament does not completely disappear after reset operation but leaves behind fractured filament fragments rich in oxygen vacancies. These oxygen vacancies undergo diffusion or re-bond with oxygen ions in the lattice upon thermal activation at ambient temperature, leading to resistance drift. Jiang et al. observed Ta-O solid solution channels and, through accelerated aging tests at high temperatures and Arrhenius fitting, determined the activation energy of this device to be as high as 1.55 eV. Based on this, they estimated its data retention time at 85°C to exceed 70,000 years [11]. Thus, the material composition of the conductive channel is critical to its drift resistance. For data requiring long-term preservation, resistive drift is clearly detrimental.

3.2 Integration Technology Issues

Despite the superior performance of memristor units, large-scale array integration technology remains under investigation. In their research on HfO_2 arrays, Chen et al. discovered an inherent trade-off between device endurance and data retention [13]. This intrinsic material-physical limitation makes it challenging to simultaneously optimize all metrics on the same process platform when designing large-scale arrays.

3.3 Complex Physical Phenomena

Currently, the complex physical phenomena within memristor structures remain poorly understood. Existing explanations for the microscopic mechanisms of resistive change are still incomplete, and achieving fully precise control over key parameters remains a challenge.

4. Future Development Trends

Intervening in ion migration and defect behavior at the nanoscale or even atomic scale through material design, particularly for the intermediate insulating layer material, represents an effective approach to addressing memristor stability issues. Recent studies indicate that nanofibrillation, bandgap engineering, superlattice engineering, and defect modulation hold promise for enhancing memristor thermal stability and electrical reliability [2]. Further investigation into ion transport, associated redox reactions, and compositional rearrangement [14] may enable more precise control over ion movement, thereby achieving finer regulation of this “resistance switch”. Furthermore, since Liu et al. developed a bismuth-doped tin oxide ($Bi{:}SnO_2$) memristor [15] that reduced the device's self-adaptive current, operating current, and switching voltage, thereby resolving issues of low uniformity [3]. Therefore, it is also expected that by doping the intermediate insulating material with specific elements, the performance of the memristor can be brought closer to the ideal state. Pan et al. significantly reduced the oxygen vacancy concentration in the TiO_2-WO_{3-X} (TWO) hybrid functional layer by doping TiO_2 into WO_{3-X} [12], thereby decreasing the number of mobile oxygen vacancies and limiting the randomness of conductive filament formation. Zhang et al. achieved precise design of charge capture and release pathways and barriers by stacking two-dimensional materials with distinct band structures, such as MoS_2/PTCDA and h-BN/WSe_2 [16], thereby reducing randomness.

Additionally, atomic-level flat interfaces can be utilized to reduce the instability of memristors. This can be achieved by constructing two-dimensional material heterojunctions. The atomically flat surfaces and absence of dangling bonds in two-dimensional materials result in minimal interface defects in van der Waals heterojunctions [16], significantly mitigating stability issues caused by interface roughness and random traps.

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